Claims:

1. A system, comprising:

a processor;

a nonvolatile mass storage device; and

a host control interface to couple the processor to the nonvolatile mass storage device and issue read/write commands to manage polarity.

2. The system of claim 1 wherein the nonvolatile mass storage device is a disk cache.

3. The system of claim 1 wherein the nonvolatile mass storage device has polymer memory devices.

4. The system of claim 3 wherein the nonvolatile mass storage device having polymer memory devices is a disk cache.

5. The system of claim 1 wherein polarity management ensures that data is stored in the nonvolatile mass storage device with a polarity opposite of that last used for a memory word.

6. The system of claim 1 wherein polarity management includes an explicit polarity control with a polarity indicator to determine data polarity for each write.

7. The system of claim 1 wherein polarity management includes a recovered polarity that uses a last polarity from a read operation for a subsequent write operation.

8. The system of claim 1 wherein polarity management includes an automatic polarity where contents of a polarity map determine polarity on reads and polarity in the polarity map is toggled for writes.

9. A computer system, comprising:

a processor;

multiple memory devices; and

a host controller interface to couple the processor to the multiple memory devices and issue a multi-control command to address the multiple memory devices with potentially different operation types.

10. The computer system of claim 9 where the multiple memory devices form a disk cache.

11. The computer system of claim 9 where the multiple memory devices are polymer memory devices.

12. The computer system of claim 9 where the multiple memory devices are flash memory devices.

13. The computer system of claim 9, wherein the multi-control command allows one command packet to be fetched, decoded and executed to provide different memory operations to the multiple memory devices.

14. The computer system of claim 9, wherein the multi-control command accesses memory words in different devices of the multiple memory devices.

15. A system comprising:

a processor;

addressable mass storage devices; and

a host controller interface to couple processor commands to the addressable mass storage devices and account for special handling needs of polymer devices in the addressable mass storage devices.

16. The system of claim 15 wherein the special handling needs include reporting a number of error corrections.

17. The system of claim 15 wherein the special handling needs include using a polarity map to determine how polarity is to be handled for a specific access.

18. The system of claim 15 wherein the special handling needs include using a timing control to specify on a per operation basis what timing should be used for read/write operations.

19. The system of claim 15 wherein the special handling needs include using dynamic addressing to write data to a location in a different segment from where the data was read in the addressable mass storage devices.

20. The system of claim 15 wherein the addressable mass storage devices represent a disk cache having multiple cache storage devices.

21. The system of claim 20 wherein the special handling needs further include storing a minimum and a maximum cache line size and metadata size.

22. A system comprising:

a processor having a transceiver coupled to dual antennas; and

a memory module coupled to the processor and including,

(a) a memory controller,

(b) storage devices to form a mass storage that is coupled to the memory controller, and

(c) a host controller coupled to the processor to provide a refresh cycle issued through an interface to the storage devices.

23. The system of claim 22 wherein the storage devices are polymer memory devices.

24. The system of claim 22 wherein the storage devices are flash memory devices.

25. The system of claim 22 wherein the memory module is a bus master device that is given a list of commands to asynchronously process.

26. The system of claim 25 wherein the list of commands are processed without involvement by the processor.

27. The system of claim 22 wherein data stored by the storage devices on the memory module is not directly accessible by processor instructions.

28. The system of claim 27 wherein the data stored by the storage devices on the memory module is copied to/from system memory.

29. A system, comprising:

a processor;

main memory coupled to the processor; and

a disk cache memory module having a programming interface capable of streaming read/write data without direct processor instruction access to storage devices on the disk cache memory module, where data stored in the storage devices is retrieved and stored in the main memory.

30. The system of claim 29, wherein the storage devices are flash devices.

31. The system of claim 29, wherein the storage devices are polymer devices.

32. The system of claim 31, wherein the polymer devices are a ferroelectric polarizable material.

33. A method including functions in a host control interface to facilitate read\write operations in a mass storage to include at least one of:

(a) providing a continuous associated command to allow a group of commands to be issued together,

(b) using a polarity map to determine how polarity is to handled for a specific access to the mass storage,

(c) using a timing control to specify on a per operation basis what timings should be used for read/write operations,

(d) using dynamic addressing to write data to a location in a different segment from where the data was read,

(e) issuing a multi-command to allow different operations to multiple storage devices in the mass storage,

(f) providing a refresh cycle,

(g) recording a number or corrections applied to the mass storage, and

(h) using a scatter gather list to correctly access data in the mass storage.

34. The method of claim 33, wherein facilitating read\write operations in the mass storage includes using the mass storage having a ferroelectric polarizable material.

35. The method of claim 33, wherein facilitating read\write operations in the mass storage includes using the mass storage having a resistive change polymer memory.

36. The method of claim 33, wherein facilitating read\write operations in the mass storage further includes facilitating read\write operations in a polymer storage.

37. The method of claim 33, wherein facilitating read\write operations in the mass storage further includes facilitating read\write operations in a disk cache.

39. The method of claim 37 further including storing a minimum and maximum cache line size and metadata size in the disk cache.

40. A method of error reporting, comprising:

providing a periodic memory refresh cycle for storage devices; and

allowing a memory controller to detect an error and interrupt the software controlling the storage devices to report a memory refresh failure.

41. The method of claim 40 further including:

incorporating Polymer Ferroelectric Memory (PFEM) devices for the storage devices.

42. The method of claim 40 wherein providing the periodic memory refresh cycle for storage devices further includes providing the periodic memory refresh cycle for cache storage devices.

43. An article comprising a machine-readable storage medium containing instructions that if executed enable a host controller interface to control read/write operations for mass storage that include at least one of:

providing a continuous list of commands to allow a group of commands to be issued together;

using a polarity map to determine how polarity is to be handled for a specific access of the mass storage;

using a timing control to specify on a per operation basis what timing should be used for read/write operations;

using dynamic addressing to write data to a location in a different segment of the mass storage from where the data was read;

issuing a multi-command to allow different operations to multiple devices in the mass storage;

providing a refresh cycle; and

reporting a number of memory error corrections.

44. The article of claim 43 wherein the mass storage is a flash memory.

45. The article of claim 43 wherein the mass storage is a polymer storage.

46. The article of claim 45 wherein the polymer storage includes a ferroelectric polarizable material.

47. The article of claim 45 wherein the polymer storage includes a resistive change polymer memory.

48. The article of claim 45 wherein the mass storage is a disk cache.